Abstract of the Disclosure

The present invention provides a semiconductor integrated circuit device easy to design timing to be provided with respect to an external memory. In the semiconductor integrated circuit device (10), a second memory controller (16) is provided outside a hard macro (12) containing a first memory controller (15). The length of a wiring (second wiring) between the second memory controller (16) and an IO pad unit (13) is set shorter than the length of a wiring (first wiring) between the first memory controller (15) and the IO pad unit (13). Further, a wiring (40) is provided which transmits a switch signal for exclusively switching the states of the first memory controller (15) and the second memory controller (16) to either one of valid and invalid states.